

## IN THE U.S. PATENT AND TRADEMARK OFFICE

The re application of SAITO et al.

Application No. 10/774,463

Filed February 10, 2004

EVALUATION WIRING PATTERN AND EVALUATION METHOD FOR EVALUATING RELIABILITY OF SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE HAVING THE SAME PATTERN

## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed sheet.

A concise explanation of the relevance of these items is that these references were discovered during any searches they or their client had made, or that they were considered in the preparation of the application.

Respectfully submitted,

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RJP/psf April 21, 2004

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\* Abstract provided for the Examiner's convenience